2020 IEEE Asian Solid-State Circuits Conference (A-SSCC)

PROGRAM BOOK

November 9-11, 2020

Online

Sponsored by

IEEE Solid-State Circuits Society (IEEE SSCS)

A-SSCC 2020 Program-at-a-glance
November 9-11, 2020 (JST, UCT+9)

Day	Date	Time(JST)	Track A	Track B	Track C	Track D	Track E
1st Day	Mon., Nov. 9	9:00-10:30	Live Tutorial I Sparsity-Aware Machine Learning Processor			**Recorded movie** SDC Exhibition/ FPGA Demo	**Recorded 1.5-min movie** presentation by regular speakers
		10:30-10:50	Break				
		10:50-12:20	Live Tutorial II Ultra-Low-Power DTC-Based Fractional-N Digital PLL Techniques				
		12:20-13:40	Lunch Break				
		13:40-15:10	Live Tutorial III Introduction to Silicon Photonics Systems and Their Modeling				
		15:10-15:30	Break				
		15:30-17:00	Live Tutorial IV Integrated Security Interface Against Cyber-Physical Attacks				
		17:00-18:45	Break				
		18:45-19:00	TPC Meeting				
2nd Day	Tue., Nov. 10	9:00-9:20	Live Opening Ceremony/ Welcome Remarks			**Recorded movie** SDC Exhibition/ FPGA Demo	**Recorded 1.5-min movie** presentation by regular speakers
		9:20-10:05	Live Session 1 - Plenary Talk 1 AI Semiconductor and Intelligent Society Kiyoung Choi, PhD, Ministry of Science and ICT, Republic of Korea				
		10:05-10:50	Live Session 1 - Plenary Talk 2 Intelligent Chips and Technologies for AIoT Era Yu-Chin Hsu, PhD, BigObject, Inc.				
		10:50-11:10	Break				
		11:10-12:25	Live Session 2 Industry Program: Low-Power Industry Solutions	Live Session 3 AI/ML Accelerators on FPGA	Live Session 4 High Resolution ADCs with Linearity Enhancement Techniques		
		12:25-13:30	Live Women-in-Circuits(WiC) & Young Professionals Joint Event				
		13:30-15:35	Live Session 5 Power Management	Live Session 6 Low-Power Digital Circuits & Systems	Live Session 7 RF & mm-Wave Chip Systems		
		15:35-15:50	Break				
		15:50-17:30	Live Session 8 - Panel What other technologies, together with circuit technology, are necessary for AIoT (AI + IoT)				
		17:30-18:30	Break				
		18:30-19:30	Live Special Q&A Session 1 (separated rooms by each session 2,3,4,5,6,&7)			Live Demo Q&A Session (separated rooms by SDC exhibition/FPGA Demo of 10)	
		19:30-21:00	Live Virtual Banquet/Award Ceremony				
3rd Day	Wed., Nov. 11	8:30-9:15	Live Session 9 - Plenary Talk 3 Co-optimization targeting future interconnection Wei Tsao, PhD, Hisilicon				**Recorded 1.5-min movie** presentation by regular oral speakers
		9:15-10:00	Live Session 9 - Plenary Talk 4 Supercomputer Fugaku - Co-designed with application developers/researchers - Toshiyuki Shimizu, Fujitsu				
		10:00-10:30	Break				
		10:30-12:35	Live Session 10 Analog Techniques	Live Session 11 RF Building Blocks	Live Session 12 Circuits and Systems for Emerging Applications		
		12:35-13:40	Lunch Break				
		13:40-15:20	Live Session 13 Bandgap and Temperature Sensors	Live Session 14 SoC for AIoT	Live Session 15 Wireline Transceiver Techniques		
		15:20-15:50	Break				
		15:50-17:30	Live Session 16 High-Speed and Low-Power Techniques for SAR-Based ADCs	Live Session 17 Biomedical & Bioinspired SoCs	Live Session 18 Intelligent Memory & AI/ML-Assisted Biomedical SoCs		
		17:30-18:30	Break				
		18:30-19:30	Live Special Q&A Session 2 (separated rooms by each session 10,11,12,13,14,15,16,17&18)				

Table of Contents

Welcome Message

On behalf of the organizing committee, it is my great pleasure to extend to you all a very warm welcome to the IEEE Asian Solid State Circuits Conference (A-SSCC) on November 9 to 11, 2020. A-SSCC is an international electronics forum that takes place in Asia with the support of the IEEE Solid State Circuits Society. From the first A-SSCC in 2005, A-SSCC 2020 will be the 16th edition of the conference where the most updated and advanced chips and circuit designs in solid-state and semiconductor fields will be presented.

Originally A-SSCC 2020 was planned to be held in Hiroshima, Japan with very strong Hiroshima Government supports. But based on the recent COVID-19 situation, the OC decides to change A-SSCC 2020 to a "virtual event". Specially to make the virtual conference more attractive, we are planning to have the "Special Q&A Sessions", "Demo Q&A Sessions" to enjoy real time interactive networking opportunities with the authors. We are also planning to have the "Virtual Banquet" that enables the interactive communication and networking among experts and students from all over the world.

The theme of A-SSCC 2020 is "Intelligent Chips for AIoT Era". The development of artificial intelligence of things (AIoT), which combines artificial intelligence (AI) and internet of things (IoT), enables new digital services to elevate customer experiences and accelerate business performance. With the advancement of solid-state circuits, intelligent chips can provide powerful computation capabilities to analyze the information through patterns, visions, and sounds. By moving part of the computing to the edge, the devices perform less time for communication, low latency, and reliable operation in offline periods. The innovations of intelligent chips will lead us to the era of AIoT.

To embrace the conference theme of A-SSCC 2020, a full and rich three-day program consisting of 4 outstanding plenary talks, 4 key technology tutorials, 1 panel discussion, 1 industry session and various regular paper sessions covering 60 regular papers in the area of analog circuits, data converters, digital circuits and systems, emerging technology and applications, memory, radio-frequency circuits, system-on-chip, and signal processing, wireline and mixed signal circuits have been organized.
The Student Design Contest and FPGA exhibition will also include "Virtual" demo session.

We are pleased to have many world-renowned experts attend this conference and share their valuable experience and knowledge with us. We hope that A-SSCC 2020 will provide valuable opportunities for scholars, students, research scientists, industrial specialists and decision makers to interact and interact with each other and create new innovations for collaboration on AIoT devices and more.

I would like to take this opportunity to express my sincere gratitude and appreciation to the members of the steering committee chaired by Prof. Hoi-Jun Yoo, the members of the technical preprogram committee chaired by Prof. Robert Chen-Hao Chang and assisted by Woogeun Rhee as Co-Chair, Po-Hung Chen as Vice-Chair for the excellent program,

the members of the organizing committee co-chaired by Dr. Satoshi Shigematsu, Dr. Masaitsu Nakajima and assisted by Dr. Koyo Nitta as Vice chair for organizing the conference even under such a very difficult situation, as well as all speakers, and authors, and sponsors.

Thank you for participating in A-SSCC 2020 again. We are confident that this conference will be a fruitful and rewarding exchange. Please enjoy it and share your positive experience with colleagues and friends. Continuous support is paramount to the continued success of A-SSCC.

Yoshifumi Okamoto
A-SSCC 2020, Conference Chair
President & COO & CTO
Socionext Inc.

Foreword

Welcome to the IEEE Asian Solid-State Circuits Conference (A-SSCC) 2020. The conference was planned to be held in Hiroshima, Japan from Nov. 9th to Nov. 11th, 2020 and became a virtual event due to COVID-19. Being one of the five conferences fully sponsored by the IEEE Solid-State Circuits Society, A-SSCC has grown to be a leading conference in the field of integrated circuits and systems design.

The conference theme for this year is “Intelligent Chips for AIoT Era.” The development of artificial intelligence of things (AIoT), which combines artificial intelligence (AI) and internet of things (IoT), enables new digital services to elevate customer experiences and accelerate business performance. With the advancement of solid-state circuits, intelligent chips can provide powerful computation capabilities to analyze the information through patterns, visions, and sounds. By moving part of the computing to the edge, the devices perform less time for communication, low latency, and reliable operation in offline periods. The innovations of intelligent chips will lead us to the era of AIoT.

This year, we received 151 submissions from 20 countries and regions around the world. Among all submissions, 87% of papers presented measurement results with silicon chips. After rigorous review process, including online meeting during July 20 - 24, the Technical Program Committee (TPC) selected 59 high quality papers from 13 countries and regions. The acceptance rate is 39%.

The conference starts with 4 tutorials on Nov. 9, 2020. Prof. Yongpan Liu, Tsinghua University presents “Sparsity-Aware Machine Learning Processor”, Prof. Kenichi Okada, Tokyo Institute of Technology presents “Ultra-Low-Power DTC-Based Fractional-N Digital PLL Techniques”, Prof. Jaeha Kim, Seoul National University presents “Introduction to Silicon Photonics Systems and Their Modeling”, Prof. Noriyuki Miura, Osaka University presents “Integrated Security Interface Against Cyber-Physical Attacks.”

Four plenary speeches are presented by distinguished scholars and industry leaders. Dr. Kiyoung Choi, Minister, Ministry of Science and ICT, Republic of Korea, shares with us his view on “AI Semiconductor and Intelligent Society” and Dr. Yu-Chin Hsu, Chairman, BigObject, Inc., Taiwan, presents “Intelligent Chips and Technologies for AIoT Era” in the morning of Nov. 10, 2020. On Nov. 11, Dr. Wei Tsao, Chief Architect & Shanghai Branch Director of Analog Design Department, Hisilicon, China, talks “Co-optimization targeting future interconnection”, and Mr. Toshiyuki Shimizu, Senior Director, Platform Development Unit, Fujitsu Limited, Japan, addresses about “Supercomputer Fugaku - Co-designed with application developers/researchers.”

A panel discussion is held on Tuesday afternoon with the topic “What other technologies, together with circuit technology, are necessary for AIoTs (AI + IoT)?”, moderated by Prof. Jerald Yoo, National University of Singapore and Prof. Milin Zhang, Tsinghua University. The panel invites experts from Intel, National University of Singapore, Samsung Electronics, National Chiao Tung University, ROHM Inc., and Tsinghua University to discuss issues related

to the key technologies to the AIoT. The industry session, held also on Tuesday, highlights advances in Low-Power Industry Solutions. Three outstanding industry papers are presented by speakers from Socionext, Samsung, and Renesas. The regular conference papers are grouped in 15 sessions in 3 parallel tracks. The Student Design Contest provides live demos from the top 9 student-authored papers including two FPGA papers. Three winners are selected and recognized at the virtual conference.

A-SSCC 2020 TPC consists of 105 members divided into 10 technical subcommittees. The members come from both industry and academia around the world. This year, TPC members gathered in virtual platform in late July to select excellent papers. Their contributions to maintain a high-quality A-SSCC are highly appreciated. Furthermore, I would like to acknowledge the leadership of the technical subcommittee chairs: Prof. Po-Chiun Huang of National Tsing Hua University (Analog Circuits and Systems), Dr. Kazuko Nishimura of Panasonic Corp. (Data Converters), Prof. Jun Zhou of University of Electronic Science and Technology of China (Digital Circuits and Systems), Dr. Chi-Cheng Ju of Mediatek (SoC and Signal Processing), Prof. Minoru Fujishima of Hiroshima University (RF), Prof. Chulwoo Kim of Korea University (Wireline and Mixed-Signal Circuits), Prof. Jerald Yoo of National University of Singapore (Emerging Technology and Applications), Dr. Junghwan Choi (Memory) of Samsung Electronics, Dr. Shigeki Tomishima of Intel (FPGA) and Dr. Stefan Rusu of TSMC (Industry Program).

I would also like to acknowledge Prof. Baoyong Chi of Tsinghua University and Prof Jung-Hoon Chun of Sungkyunkwan University, and Prof. Leibo Liu of Tsinghua University for organizing the Student Design Contest, Prof. Zhihua Wang of Tsinghua University for preparing the plenary program and panel, and Prof. Seonghwan Cho of KAIST for the tutorial planning.

I would like to extend my sincere appreciation to all authors and speakers, conference organizers, committee members, moderators, panelists, and, last but not least, all the participants. I hope you will enjoy the technical program of A-SSCC 2020, take this opportunity to network with experts around the world, and bring back good memories with you!

Robert Chang

Robert Chen-Hao Chang
Technical Program Committee Chair of A-SSCC 2020
National Chung Hsing University, Taiwan

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Plenary Sessions

Tuesday, November 10

Plenary Talk I 9:20-10:05

Digital Innovation and AI semiconductor in the AI and Post-Corona era

Kiyoung Choi, PhD
Minister, Ministry of Science and ICT, Republic of Korea

Abstract: The world is facing enormous changes caused by disruptive digital technologies such as Artificial Intelligence and big data. In particular, the significant changes of economic and social structures such as accelerated digital transformation and growth of contactless industries due to COVID-19 are actually opportunities to reconfirm the importance of digital capabilities. In this speech, I would like to present the direction of national digital innovation in the era of artificial intelligence and post-corona, based on the 'AI National Strategy' and 'Digital New Deal' policies being pursued by the Korean government.
In addition, I will discuss the importance of AI semiconductor, which is a key foundation that determines the competitiveness of AI and data ecosystems, and is growing as a new semiconductor paradigm in the AI era. Also, I will share with participants about Korea's new challenges to foster AI semiconductors.

Biography: Since September 2019, Kiyoung Choi has been serving as the Minister of Science and ICT, which is in charge of formulating policies in the 4th Industrial Revolution as well as the fields of science and ICT.
Prior to his current position, Mr. Choi was professor of the Department of Electrical and Computer Engineering, Seoul National University from 1991 to 2019. During that time, he served as Chief Vice President of the Institute of Semiconductors Engineers and as Director of Neural Processing Research Center and Embedded Systems Research Center at Seoul National University. From 1989 to 1991, he was with Cadence Design Systems, Inc., USA.
Mr. Choi received the Ph.D. degree in electrical engineering from Stanford University, USA, in 1989, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology in 1980, and the B.S. degree in electronics engineering from Seoul National University in 1978.

Plenary Sessions

Tuesday, November 10

Plenary Talk II 10:05-10:50

Intelligent Chips and Technologies for AIoT Era

Yu-Chin Hsu, PhD
Chairman, BigObject, Inc.

Abstract: The re-emergence of AI in 2016 has greatly influenced the needs for computing. It is estimated the amount of computing used in the largest AI training runs grew more than 300,000x from 2012 to 2018. Roughly, it doubles every 3.5 months. Semiconductor industry will continue to be important in the new era. Foreseeing the coming of AI and data age, in Taiwan we initiated several major programs in AI in 2017. For AI edge computing, we focus on six major areas: (1) advanced sensors, circuits and systems. (2) next generation memory design. (3) neuromorphic computing and AI chip. (4) security for Internet of thing. (5) UAV components, circuits and systems. (6) advanced semiconductor process, material, and components. In this presentation, we review the overall plan for the AI edge computing program, and present some of the results that has been published. We anticipate the industry will be benefit from the talents being cultivated and the results to be applied in industrial applications.

Biography: Dr. Hsu has more than 30 years of experience in the EDA. He found NexSyn Inc. which was merged into Avant! in 1995, and co-found Novas Inc. (part of SpringSoft) in 1999, and was merged into Synopsys in 2012. He served in senior management roles in Avant!, SpringSoft, and Synopsys.
He held faculty position in Tsing-Hua University, Taiwan, and University of California, Riverside, USA.
Dr. Hsu was appointed as Debuty Minister of Ministry of Science and Technology, Taiwan, from 2017.04-2020.05. During his tenure, he helped initiating the artificial intelligence(AI) strategic programs and semiconductor for AI programs in Taiwan. He also managed the academia-industrial collaboration programs, Science Park, and entrepreneurship and innovation ecosystem.
Dr. Hsu holds a B.S. from the National Taiwan University, and an M.S. and a Ph.D. from the University of Illinois Urbana-Champaign.

Plenary Sessions

Wednesday, November 11

Plenary Talk III 8:30-9:15

Co-optimization targeting future interconnection

Wei Tsao, PhD
Chief Architect & Shanghai Branch Director of Analog Design Department, Hisilicon

Abstract: The future interconnection techniques should satisfy greater bandwidth, less latency, and higher energy efficiency for both out-of-chip and inside-chip scenarios; while the engineering constraints and cost-performance trade-off on channel characteristics, modulation/coding technique, and analog-digital transceiver scheme, must restrict the fulfilment of interconnection design target. In order to attain the destination mentioned above, co-optimization is employed toward channel, modulation/coding, and transceiver scheme. In this paper, the requirement for future interconnection, channel situation, and some implementation trends are presented.

Biography: Dr. Wei Tsao is currently Chief Architect and Shanghai Branch Director of Analog Design Department, Hisilicon Inc., responsible for architecture competitiveness of Hisilicon analog-digital mixed IP, and in charge of analog development team in Shanghai. He joined in Hisilicon in 2009, and has delivered many key analog-digital mixed IP for Huawei products, including the Ethernet PHY, High Bandwidth Memory interface PHY, Ultra-high speed converters, PCIE SerDes etc. Before joining Hisilicon, Dr. Wei Tsao has mixed signal chip development and management experiences in high-speed interconnect PHY/SerDes area for storage and communication products, with several companies in US. He has worked as architect in mixed signal area for 20 years.
Dr. Wei Tsao has published more than 10 papers in journals and conferences, he has many China and US patents as first or co-inventor. His current main interest is in Ultra-high speed physical layer technique, mixed signal system architecture and automotive mixed signal chip solution. Dr. Wei Tsao received his BS and PhD from Shanghai Jiaotong University.

Plenary Sessions

Wednesday, November 11

Plenary Talk IV 9:15-10:00

Supercomputer Fugaku - Co-designed with application developers/researchers -

Mr. Toshiyuki Shimizu
Senior Director, Platform Development Unit,
Fujitsu Limited

Abstract: Supercomputer FUGAKU has been developed through co-design efforts with application developers/researchers and system-software/hardware designers. The design targets of Fugaku were high application execution efficiency, low-power consumption, and ease of use. In this paper, the Fugaku architecture and evaluation results are briefly explained.
Performance estimations of target applications in the design phase and using real hardware are compared.

Biography: Mr. Toshiyuki Shimizu is Senior Director, Platform Development Unit, at Fujitsu Limited. Mr. Shimizu has been deeply and continuously involved in the development of scalar parallel supercomputers, large SMP enterprise servers, and x86 cluster systems. His primary research interest is in interconnect architecture, most recently culminating in the development of the Tofu interconnect for the K computer and PRIMEHPC series.
He leads the development of Fujitsu's high-end supercomputer PRIMEHPC series and the Fugaku supercomputer formerly known as Post-K. Mr. Shimizu received his Masters of Computer Science degree from Tokyo Institute of Technology in 1988.

Tutorial Session

Monday, November 9

TUTORIAL I 9:00-10:30

Sparsity-Aware Machine Learning Processor

Prof. Yongpan Liu
Tsinghua Univ.

Abstract: Sparsity is widely existed in modern neural networks and how to support such sparsity in hardware is an important direction to enhance energy efficiency of machine learning chips. This tutorial will first begin with an introduction of various pruning algorithm techniques to achieve sparse neural network (i.e. unstructured and structured sparse networks). Furthermore, we review different up-to-date architectures and chips to make efficient inference and training of sparse neural network, covering both spatial domain as well as time domain sparsity. Finally, we discuss challenges and future directions to support sparsity in computing-in-memory artificial intelligent chips.

Biography: Yongpan Liu received the B.S., M.S., and Ph.D. degrees from the Electronic Engineering Department, Tsinghua University, Beijing, China, in 1999, 2002, and 2007, respectively. He was a Visiting Scholar with Pennsylvania State University, and the City University of Hong Kong. He is currently an Associate Professor with the Department of Electronic Engineering, Tsinghua University. Prof. Liu is a Program Committee Member for DAC, DATE, ASP-DAC, ISLPED, ICCD, and A-SSCC. He has received under 40 Young Innovators Award DAC 2017, Micro Top Pick 2016, the Best Paper Award from ASPDAC2017, HPCA 2015, and Design Contest Awards of ISLPED in 2012 and 2013. He served as the General Chair for AWSSS 2016 and IWCR 2018 and the Technical Program Chair for NVMSA 2019. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II, and the IET Cyber-Physical Systems.

Tutorial Session

Monday, November 9

TUTORIAL II 10:50-12:20

Ultra-Low-Power DTC-Based Fractional-N Digital PLL Techniques

Prof. Kenichi Okada
Tokyo Inst. of Tech.

Abstract: In this tutorial, some design techniques for fractional-N digital PLL will be introduced to improve both jitter and power consumption especially for low-power applications. A highly-linear and low-power DTC and TDC will be presented as well as system-level optimization. An isolated constant-slope DTC realizes 10bit 0.1mW operation with 26MHz reference clock, and sub-ps INL is achieved. The DTC-based AD-PLL achieves FoM of -246dB with 0.98mW power consumption and -56dBc worst-case fractional spur. For further power saving, duty-cycled FLL, sub-sampling/sampling switching, charge-recycling DTC, and transformer-based DCO for impedance peaking will be also explained, which achieves 0.265mw power consumption with FoM of -237dB at 2.4GHz. Finally, a DPLL-based ADC and a BLE transceiver using DPLL will be introduced.

Biography: Kenichi Okada received the B.E., M.E., and Ph.D. degrees in Communications and Computer Engineering from Kyoto University in 1998, 2000, and 2003, respectively. From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science in Kyoto University. In 2003, he joined Tokyo Institute of Technology where he is now a Professor of Electrical and Electronic Engineering. He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011 and Best Design Award in 2014 and 2015, the RFIC Symposium Best Student Paper Award in 2019, the Kenjiro Takayanagi Achievement Award in 2020, the IEEE CICC Best Paper Award in 2020. He is/was a member of the technical program committees of IEEE International Solid-State Circuits Conference (ISSCC), VLSI Circuits Symposium, European Solid-State Circuits Conference (ESSCIRC), Radio Frequency Integrated Circuits Symposium (RFIC), and he also is/was Guest Editors and an Associate Editor of IEEE Journal of Solid-State Circuits (JSSC), an Associate Editor of IEEE Transactions on Microwave Theory and Techniques (T-MTT), a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).

Tutorial Session

Monday, November 9

TUTORIAL III 13:40-15:10

Introduction to Silicon Photonics Systems and Their Modeling

Prof. Jaeha Kim
Seoul National Univ.

Abstract: Silicon photonics systems integrate photonic components such as optical waveguides, coupler, resonator, etc. along with electronic components on the same silicon chip to realize high-bandwidth, high-density, and low-power communication. This tutorial provides an overview on common photonic devices such as microring modulator, Mach-Zehnder modulator, electro-absorption modulator, etc, and demonstrates how to model various wavelength-division multiplexing (WDM) systems tightly interacting with analog or digital electronic components and simulate them efficiently in SystemVerilog.

Biography: Jaeha Kim received the B.S. degree in electrical engineering from Seoul National University in 1997, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1999 and 2003, respectively. From 2001 to 2003, he was with True Circuits, Inc., USA, as a Circuit Designer. He was with Rambus Inc. as a Principal Engineer from 2006 to 2009, Stanford University as an Acting Assistant Professor from 2009 to 2010. In 2010, he joined Seoul National University, where he is currently an Associate Professor. In 2015, he founded Scientific Analog, Inc., an EDA company involved in analog/mixed-signal verification. Prof. Kim served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC), the Custom Integrated Circuits Conference (CICC), the International Conference on Computer-Aided Design, and the Asian Solid-State Circuit Conference (A-SSCC). He was cited as a Top 100 Technology Leader of Korea in 2020 by the National Academy of Engineering of Korea. He was a recipient of the Takuo Sugano Award for Outstanding Far-East Paper at the 2005 International Solid State Circuits Conference (ISSCC) and the Low Power Design Contest Award at the 2001 International Symposium on Low Power Electronics and Design.

Tutorial Session

Monday, November 9

TUTORIAL IV 15:30-17:00

Integrated Security Interface Against Cyber-Physical Attacks

Prof. Noriyuki Miura
Osaka University

Abstract: The continuous growth in computing technology emerges various advanced information services today. The information managed in such services is becoming increasingly critical and hence valuable for malicious attackers. In order to steal, destroy, or manipulate such information in a cyber domain, the attackers exploits security holes in a physical domain computing entity i.e. IC hardware. This so-called cyber-physical attacks are currently one of the most serious security threats in realizing future advanced information society where the information security is the-root-of-trust of all the critical services such as autonomous driving, drone guard, and robot nursing. This tutorial lecture will cover several key countermeasures namely integrated security interface against the cyber-physical attacks, including 1) power/EM side-channel, 2) EM/laser fault-injection, 3) chip-package-board hardware counterfeiting, and 4) sensor spoofing attacks. Future perspectives on the information security in the next-generation society will also be covered.

Biography: Noriyuki Miura received the B.S., M.S., and Ph.D. degrees in electrical engineering all from Keio University, Yokohama, Japan. From 2005 to 2008, he was a JSPS Research Fellow and since 2007 an Assistant Professor with Keio University, where he developed wireless interconnect technology for 3D integration. In 2012, he moved to Kobe University, Kobe, Japan, and became a Professor at Osaka University, Suita, Japan in 2020. Also, he was concurrently appointed as a JST PRESTO researcher, and now working on hardware security/safety and next-generation heterogeneous computing systems. Prof. Miura is currently serving as a Technical Program Committee (TPC) Member for A-SSCC and Symposium on VLSI Circuits. He served as the TPC Vice Chair of 2015 A-SSCC. He was a recipient of the Top ISSCC Paper Contributors 2004-2013, the IACR CHES Best Paper Award in 2014.

Student Design Contest (SDC) Exhibition/ FPGA Demo

Monday, November 9

9:00-17:00, November 9 Pre-recorded presentation movie
9:00-18:30, November 10 Pre-recorded presentation movie
18:30-19:30, November 10 Interactive Q&A Session by each demo

SDC 1/FPGA Demo S3-1 (1157)
An Energy-Efficient GAN Accelerator with On-Chip Training for Domain Specific Optimization
Soyeon Kim, Sanghoon Kang, Donghyeon Han, Sangyeob Kim, Sangjin Kim, Hoi-Jun Yoo
KAIST, Korea

SDC 2/FPGA Demo S3-2 (1039)
A 112-765 GOPS/W FPGA-Based CNN Accelerator Using Importance Map Guided Adaptive Activation Sparsification for Pix2pix Applications
Wenyu Sun, Chen Tang, Zhuqing Yuan, Zhe Yuan, Huazhong Yang, Yongpan Liu
Tsinghua University, China

SDC 3 S7-1 (1153)
A W-Band 4 GHz-BW Multi-User Interference-Tolerant Radar with 28-nm CMOS Front-Ends
Rulin Huang{2}, Ching-Wen Chiang{1}, Chia-Jen Liang{1}, Yanghyo Kim{2}, Yen-Cheng Kuan{1}, Mau-Chung Chang{2}
{1}National Chiao Tung University, Taiwan; {2}University of California, Los Angeles, United States

SDC 4 S11-2 (1115)
Digital Evolution of the Quadrature Balanced Power Amplifier Transceiver for Full Duplex Wireless
Nimrod Ginzberg{1}, Dror Regev{2}, Emanuel Cohen{1}
{1}Technion - Israel Institute of Technology, Israel; {2}Toga Networks, a Huawei Company, Israel

SDC 5 S12-2 (1079)
A Power-Efficient Current Readout Circuit with VCO-Based 2nd-Order CT ΔΣ ADC for Electrochemistry Acquisition
Hao-Yun Lee, Peng-Wei Huang, Ding-Siang Ciou, Zhan-Xian Liao, Shuenn-Yuh Lee
National Cheng Kung University, Taiwan

SDC 6 S13-2 (1065)
A 0.14 pJ/Conversion Fully Energy-Autonomous Temperature-to-Time Converter for Biomedical Applications

Joanne Si Ying Tan, Jeong Hoan Park, Jiamin Li, Yilong Dong, Kwok Hoe Chan, Ghim Wei Ho, Jerald Yoo
National University of Singapore, Singapore

SDC 7 S14-1 (1002)
Fully-Synthesizable All-Digital Unified Dynamic Entropy Generation, Extraction and Utilization Within the Same Cryptographic Core
Sachin Taneja, Massimo Alioto
National University of Singapore, Singapore

SDC 8 S16-1 (1061)
A 65.5dB SNDR 8.1-11.1nW ECG SAR ADC with Adaptive Latching OSC Based Comparator and DAC Calibration
Kejin Li, Wai-Hong Zhang, Yan Zhu, Chi-Hang Chan, Rui Paulo Martins
University of Macau, Macau

SDC 9 S18-3 (1078)
Wireless Charging EEG Monitoring SoC with AI Algorithm-Driven Electrical and Optogenetic Stimulation for Epilepsy Control
Zhan-Xian Liao{2}, Yao-Tse Chang{2}, Chieh Tsou{2}, Po-Hao Cheng{2}, Hao-Yun Lee{2}, Peng-Wei Huang{2}, Shuenn-Yuh Lee{2}, Chou-Ching Lin{3}, Gia-Shing Shieh{1}
{1}Ministry of Health and Welfare Tainan Hospital, Taiwan; {2}National Cheng Kung University, Taiwan; {3}National Cheng Kung University Hospital, Taiwan

FPGA Demo 10 S3-3 (1122)
An Energy-Efficient Multi-Core Restricted Boltzmann Machine Processor with On-Chip Bio-Plausible Learning and Reconfigurable Sparsity
Jiajun Wu{1}, Xuan Huang{1}, Le Yang{1}, Liang Wang{1}, Jipeng Wang{1}, Zuozhu Liu{3}, Kwen-Siong Chong{2}, Shaowei Lin{4}, Chao Wang{1}
{1}Huazhong University of Science and Technology, China; {2}Nanyang Technological University, Singapore; {3}National University of Singapore, Singapore; {4}Singapore University of Technology and Design, Singapore

Program Schedule

Tuesday, November 10

Opening Ceremony

Session date and time: 9:00 - 9:20, November 10, 2020

Tuesday, November 10

S1 Session: Plenary Talk 1

Session date and time: 9:20 - 10:05, November 10, 2020

Session Chair: Robert Chen-Hao Chang, National Chung Hsing University

S1-1

Digital Innovation and AI semiconductor in the AI and Post-Corona era

Kiyoung Choi, PhD, Ministry of Science and ICT, Republic of Korea

Tuesday, November 10

S1 Session: Plenary Talk 2

Session date and time: 10:05 - 10:50, November 10, 2020

Session Chair: Robert Chen-Hao Chang, National Chung Hsing University

S1-2

Intelligent Chips and Technologies for AIoT Era

Yu-Chin Hsu, PhD, BigObject, Inc.

Tuesday, November 10

S2 Session: Low-Power Industry Solutions

Session date and time: 11:10 - 12:25, November 10, 2020

Session Chairs: Yi Kang, Univ. of Science and Technology/Saki Hatta, Nippon Telegraph and Telephone

S2-1 (1118) 11:10-11:35

A 12.1 TOPS/W Mixed-Precision Quantized Deep Convolutional Neural Network Accelerator for Low Power on Edge / Endpoint Device

Takanori Isono, Makoto Yamakura, Satoshi Shimaya, Isao Kawamoto, Nobuhiro Tsuboi, Masaaki Mineo, Wataru Nakajima, Kenichi Ishida, Shin Sasaki, Toshio Higuchi, Masahiro Hoshaku, Daisuke Murakami, Toshifumi Iwasaki, Hiroshi Hirai
Socionext Inc, Japan

S2-2 (1036) 11;35-12:00

A 2.68mW/Gbps, 1.62-8.1Gb/s Receiver for Embedded DisplayPort Version1.4b to Support 14dB Channel Loss

Gunjan Mandal, Sunil Rajan, Sanjeeb Kumar Ghosh, Saikat Hazra, Raghavendra Molthati, Parin Rajnikant Bhuta, Santosh Kumar Reddy, Vishnu Kalyanamahadevi Gopalan J, Sumanth Chakkirala, Avneesh Singh Verma, Umamaheswara Reddy Katta, Venugopal Sadana, Dayakar Bethi, Abul Hassan Savanur, Praveen S Bharadwaj, Krupal Jitendra Mehta, Kuntal Pandya
Samsung Semiconductor India Research, India

S2-3 (1007) 12:00-12:25

A High-Precision Analog Front End Integrated in a 32bit Microcontroller for Industrial Sensing Applications

Koji Yoichi, Sugako Otani, Kazutoshi Tsuda, Naoya Tokimoto, Hideki Kamegawa, Yoshihisa Satou, Shioto Tanaka, Hideki Otsu, Mitsuru Hiraki, Masao Ito, Mitsuya Fukazawa, Hiroyuki Kondo
Renesas Electronics Corporation, Japan

Tuesday, November 10

S3 Session: AI/ML Accelerators on FPGA

Session date and time: 11:10 - 12:25, November 10, 2020

Session Chairs: Ji-Hoon Kim, Ewha Womans University/Yong-Pan Liu. Tsinghua University

S3-1 (1157) 11:10-11:35

An Energy-Efficient GAN Accelerator with On-Chip Training for Domain Specific Optimization

Soyeon Kim, Sanghoon Kang, Donghyeon Han, Sangyeob Kim, Sangjin Kim, Hoi-Jun Yoo
KAIST, Korea

S3-2 (1039) 11:35-12:00

A 112-765 GOPS/W FPGA-Based CNN Accelerator Using Importance Map Guided Adaptive Activation Sparsification for Pix2pix Applications

Wenyu Sun, Chen Tang, Zhuqing Yuan, Zhe Yuan, Huazhong Yang, Yongpan Liu
Tsinghua University, China

S3-3 (1122) 12:00-12:25

An Energy-Efficient Multi-Core Restricted Boltzmann Machine Processor with On-Chip Bio-Plausible Learning and Reconfigurable Sparsity

Jiajun Wu{1}, Xuan Huang{1}, Le Yang{1}, Liang Wang{1}, Jipeng Wang{1}, Zuozhu Liu{3}, Kwen-Siong Chong{2}, Shaowei Lin{4}, Chao Wang{1}
{1}Huazhong University of Science and Technology, China; {2}Nanyang Technological University, Singapore; {3}National University of Singapore, Singapore; {4}Singapore University of Technology and Design, Singapore

Tuesday, November 10

S4 Session: High Resolution ADCs with Linearity Enhancement Techniques

Session date and time: 11:10 - 12:00, November 10, 2020

Session Chairs: Yan Zhu, University of Macau/Sanroku Tsukamoto, Fujitsu Laboratories Ltd.

S4-1 (1095) 11:10-11:35

An Input Insensitive Quantization Error Extraction Circuit for 8MHz-BW 79dB-DR CT MASH ﾎ采」ADC with Multi-Rate LMS-Based Background Calibration

Mitsuya Fukazawa, Masaki Fujiwara, Atsushi Ochi, Raed Alsubaie, Tetsuo Matsui
Renesas Electronics Corporation, Japan

S4-2 (1111) 11:35-12:00

A 16b 1.62MS/s Calibration-Free SAR ADC with 86.6dB SNDR Utilizing DAC Mismatch Cancellation Based on Symmetry

Shota Konno, Yuichi Miyahara, Kazuki Sobue, Koichi Hamashita
Asahi Kasei Microdevices Corp., Japan

Tuesday, November 10

Special Session: Women-in-Circuits (WiC) & Young Professionals Joint Event

Session date and time: 12:25 - 13:30, November 10, 2020

Session Chairs: Milin Zhang, Tsinghua University/Zeynep Lulec, Analog Devices

Three separated rooms will be provided by topics. Select the room and join the live discussion.

Topics:
Room 1) what is my advisor talking about every day?
Room 2) what does the life look like in academia?
Room 3) How to find a good job in industry?

Tuesday, November 10

S5 Session: Power Management

Session date and time: 13:30 - 15:35, November 10, 2020

Session Chairs: Makoto Takamiya, University of Tokyo/Hyun-Sik Kim, KAIST

S5-1 (1032) 13:30-13:55

Transient Output-Current Regulator with Background Calibration Applied to a Buck Converter for Fast Load-Transient Response

Yi-Wei Huang, Ting-Yu Yu, Tai-Haur Kuo
National Cheng Kung University, Taiwan

S5-2 (1087) 13:55-14:20

A 2-Phase 3-Level Buck DC-DC Converter with X-Connected Flying Capacitors for Current Balancing

Chuang Wang, Yan Lu, Mo Huang, Rui Paulo Martins
University of Macau, China

S5-3 (1135) 14:20-14:45
A Redistributable Capacitive Power Converter for Indoor Light-Powered Batteryless IoT Devices
Hao-Chung Cheng, Yu-Tong Su, Po-Han Chen, Po-Hung Chen
National Chiao Tung University, Taiwan

S5-4 (1126) 14:45-15:10
Input-Adaptive and Regulated Multi-Output Power Management Unit for Wireless Power Reception and Distribution in Multi-Unit Implantable Devices
Unbong Lee, Doojin Jang, Wanyeong Jung, Minkyu Je
KAIST, Korea

S5-5 (1107) 15:10-15:35
A 6.78-MHz Single-Stage Regulating Rectifier with Hysteretic Control and Current-Wave Modulation
Jie Lin{1}, Chenchang Zhan{1}, Yan Lu{2}
{1}Southern University of Science and Technology, China; {2}University of Macau, Macau

Tuesday, November 10

S6 Session: Low-Power Digital Circuits & Systems

Session date and time: 13:30 - 15:10, November 10, 2020

Session Chairs: Taejoong Song, Samsung Electronics/Yoonmyung Lee, Sungkyunkwan University

S6-1 (1057) 13:30-13:55
A Time-Domain Computing-in-Memory Based Processor Using Predictable Decomposed Convolution for Arbitrary Quantized DNNs
Jianxun Yang{3}, Yuyao Kong{2}, Zhao Zhang{3}, Zhuangzhi Liu{3}, Jing Zhou{3}, Yiqi Wang{3}, Yonggang Liu{3}, Chenfu Guo{3}, Te Hu{3}, Congcong Li{3}, Leibo Liu{3}, Jin Zhang{1}, Shaojun Wei{3}, Jun Yang{2}, Shouyi Yin{3}
{1}Ingenic Semiconductor CO, China; {2}Southeast University, China; {3}Tsinghua University, China

S6-2 (1017) 13:55-14:20
A Redundancy Eliminated Flip-Flop in 28nm for Low-Voltage Low-Power Applications
Gicheol Shin, Eunyoung Lee, Jongmin Lee, Yongmin Lee, Yoonmyung Lee
Sungkyunkwan University, Korea

S6-3 (1006) 14:20-14:45
Voice Activity Detection with >83% Accuracy Under SNR Down to -3dB at 1.19μW and 0.07mm² in 40nm
Jing Horng Teo, Karim Ali, Massimo Alioto
National University of Singapore, Singapore

S6-4 (1052) 14:45-15:10
A μProcessor Layer for mm-Scale Die-Stacked Sensing Platforms Featuring Ultra-Low Power Sleep Mode at 125˚C
Jeongsup Lee{3}, Yejoong Kim{3}, Minchang Cho{3}, Makoto Yasuda{2}, Satoru Miyoshi{1}, Masaru Kawaminami{2}, David Blaauw{3}, Dennis Sylvester{3}
{1}Fujitsu Electronics America, Inc., United States; {2}United Semiconductor Japan Co., Ltd., Japan; {3}University of Michigan, United States

Tuesday, November 10

S7 Session: RF & mm-Wave Chip Systems

Session date and time: 13:30 - 15:35, November 10, 2020

Session Chairs: Minjae Lee, Gwangju Institute of Science and Technology/Bo Zhao, Zhejiang University

S7-1 (1153) 13:30-13:55

A W-Band 4 GHz-BW Multi-User Interference-Tolerant Radar with 28-nm CMOS Front-Ends

Rulin Huang{2}, Ching-Wen Chiang{1}, Chia-Jen Liang{1}, Yanghyo Kim{2}, Yen-Cheng Kuan{1}, Mau-Chung Chang{2}

{1}National Chiao Tung University, Taiwan; {2}University of California, Los Angeles, United States

S7-2 (1069) 13:55-14:20

An 800-Ps Origami True-Time-Delay-Based CMOS Receiver Front End for 6.5-9 GHz Phased Arrays

Min Li{2}, Nayu Li{2}, Huiyan Gao{2}, Zijiang Zhang{2}, Shaogang Wang{2}, Yen-Cheng Kuan{1}, Xiaopeng Yu{2}, Zhiwei Xu{2}

{1}National Chiao Tung University, Taiwan; {2}Zhejiang University, China

S7-3 (1143) 14:20-14:45

A Ka-Band CMOS 4-Beam Phased-Array Receiver with Symmetrical Beam-Distribution Network

Na Peng, Peng Gu, Xiaohu You, Dixian Zhao

Southeast University, China

S7-4 (1003) 14:45-15:10

287-GHz CMOS Transceiver Pixel Array in a QFN Package for Active Imaging

Pranith Reddy Byreddy{2}, Yukun Zhu{2}, Harshpreet Singh Bakshi{2}, Kenneth K O{2}, Wooyeol Choi{1}

{1}Oklahoma State University, United States; {2}University of Texas at Dallas, United States

S7-5 (1024) 15:10-15:35

A 5 dBm 30.6% Efficiency 915 MHz Transmitter with 210 µW ULP PLL Employing Frequency Tripler and Digitally Controlled Duty/Phase Calibration Buffer

Kyung-Sik Choi{1}, Keun-Mok Kim{1}, Jinho Ko{2}, Sang-Gug Lee{1}

{1}KAIST, Korea; {2}Phychips Inc., Korea

Tuesday, November 10

S8 Session: Panel Session: What other technologies, together with circuit technology, are necessary for AIoT (AI + IoT)

Session date and time: 15:50 - 17:30, November 10, 2020

Moderators:	Jerald Yoo	National University of Singapore
	Milin Zhang	Tsinghua University
Panelists:	Shigeki Tomishima	Intel
	Massimo Alioto	National Univ. of Singapore
	Sukhwan Lim	Samsung Electronics
	Chen-Yi Lee	National Chiao Tung Univ.
	Yoshinori Miyamae	ROHM Inc.
	Hanjun Jiang	Tsinghua Univ.

Tuesday, November 10

Special Q&A Session

Session date and time: 18:30 - 19:30, November 10, 2020

This session provides all participants an opportunity to verbally with the authors in the virtual rooms separated by sessions of S2 through S7 on November 10.
The track E which shows 1.5-minute summary presentation helps to give essence of each presentation for those who do not listen to the presentations on that day,
All authors of the following sessions join their rooms.

S2 Low-Power Industry Solutions
S3 AI/ML Accelerators on FPGA
S4 High Resolution ADCs with Linearity Enhancement Techniques
S5 Power Management
S6 Low-Power Digital Circuits & Systems
S7 RF & mm-Wave Chip Systems

Tuesday, November 10

Student Design Contest (SDC) Exhibition/ FPGA Demo

Session date and time: 18:30 - 19:30, November 10, 2020

This session provides all participants an opportunity to communicate verbally with the authors of Student Design Contest in the virtual rooms separated by paper/demo.
Take a look at the track D which shows 3-minute demo presentation.

SDC 1/FPGA Demo S3-1 (1157)
An Energy-Efficient GAN Accelerator with On-Chip Training for Domain Specific Optimization
Soyeon Kim, Sanghoon Kang, Donghyeon Han, Sangyeob Kim, Sangjin Kim, Hoi-Jun Yoo
KAIST, Korea

SDC 2/FPGA Demo S3-2 (1039)
A 112-765 GOPS/W FPGA-Based CNN Accelerator Using Importance Map Guided Adaptive Activation Sparsification for Pix2pix Applications
Wenyu Sun, Chen Tang, Zhuqing Yuan, Zhe Yuan, Huazhong Yang, Yongpan Liu
Tsinghua University, China

SDC 3 S7-1 (1153)
A W-Band 4 GHz-BW Multi-User Interference-Tolerant Radar with 28-nm CMOS Front-Ends
Rulin Huang{2}, Ching-Wen Chiang{1}, Chia-Jen Liang{1}, Yanghyo Kim{2}, Yen-Cheng Kuan{1}, Mau-Chung Chang{2}
{1}National Chiao Tung University, Taiwan; {2}University of California, Los Angeles, United States

SDC 4 S11-2 (1115)
Digital Evolution of the Quadrature Balanced Power Amplifier Transceiver for Full Duplex Wireless
Nimrod Ginzberg{1}, Dror Regev{2}, Emanuel Cohen{1}
{1}Technion - Israel Institute of Technology, Israel; {2}Toga Networks, a Huawei Company, Israel

SDC 5 S12-2 (1079)
A Power-Efficient Current Readout Circuit with VCO-Based 2nd-Order CT ΔΣ ADC for Electrochemistry Acquisition
Hao-Yun Lee, Peng-Wei Huang, Ding-Siang Ciou, Zhan-Xian Liao, Shuenn-Yuh Lee
National Cheng Kung University, Taiwan

SDC 6 S13-2 (1065)
A 0.14 pJ/Conversion Fully Energy-Autonomous Temperature-to-Time Converter for Biomedical Applications
Joanne Si Ying Tan, Jeong Hoan Park, Jiamin Li, Yilong Dong, Kwok Hoe Chan, Ghim Wei Ho, Jerald Yoo
National University of Singapore, Singapore

SDC 7 S14-1 (1002)
Fully-Synthesizable All-Digital Unified Dynamic Entropy Generation, Extraction and Utilization Within the Same Cryptographic Core
Sachin Taneja, Massimo Alioto
National University of Singapore, Singapore

SDC 8 S16-1 (1061)
A 65.5dB SNDR 8.1-11.1nW ECG SAR ADC with Adaptive Latching OSC Based Comparator and DAC Calibration
Kejin Li, Wai-Hong Zhang, Yan Zhu, Chi-Hang Chan, Rui Paulo Martins
University of Macau, Macau

SDC 9 S18-3 (1078)
Wireless Charging EEG Monitoring SoC with AI Algorithm-Driven Electrical and Optogenetic Stimulation for Epilepsy Control
Zhan-Xian Liao{2}, Yao-Tse Chang{2}, Chieh Tsou{2}, Po-Hao Cheng{2}, Hao-Yun Lee{2}, Peng-Wei Huang{2}, Shuenn-Yuh Lee{2}, Chou-Ching Lin{3}, Gia-Shing Shieh{1}
{1}Ministry of Health and Welfare Tainan Hospital, Taiwan; {2}National Cheng Kung University, Taiwan; {3}National Cheng Kung University Hospital, Taiwan

FPGA Demo 10 S3-3 (1122)
An Energy-Efficient Multi-Core Restricted Boltzmann Machine Processor with On-Chip Bio-Plausible Learning and Reconfigurable Sparsity
Jiajun Wu{1}, Xuan Huang{1}, Le Yang{1}, Liang Wang{1}, Jipeng Wang{1}, Zuozhu Liu{3}, Kwen-Siong Chong{2}, Shaowei Lin{4}, Chao Wang{1}
{1}Huazhong University of Science and Technology, China; {2}Nanyang Technological University, Singapore; {3}National University of Singapore, Singapore; {4}Singapore University of Technology and Design, Singapore

Tuesday, November 10

Virtual Banquet/Award Ceremony

Session date and time: 19:30 - 21:00, November 10, 2020

Wednesday, November 11

S9 Session: Plenary Talk 3

Session date and time: 8:30 - 9:15, November 11, 2020

Session Chair: Woogeun Rhee, Tsinghua University

Co-Optimization Targeting Future Interconnection
Wei Tsao
HiSilicon Technologies Co., Ltd,, China

Wednesday, November 11

S9 Session: Plenary Talk 4

Session date and time: 9:15 - 10:00, November 11, 2020

Session Chair: Woogeun Rhee, Tsinghua University

Supercomputer Fugaku - Co-designed with application developers/researchers -
Toshiyuki Shimizu, Fujitsu

Wednesday, November 11

S10 Session: Analog Techniques

Session date and time: 10:30 – 12:10, November 11, 2020

Session Chairs: Michael Choi, Samsung/ Vanessa Chen,Carnegie Mellon University

S10-1 (1148) 10:30-10:55
A 0.45/0.2 NEF/PEF 12 nV/√Hz Highly Configurable Discrete-Time Low-Noise Amplifier
Gabriele Atzeni, Alessandro Novello, Giorgio Cristiano, Jiawei Liao, Taekwang Jang
ETH Zurich, Switzerland

S10-2 (1134) 10:55-11:20
A 0.5-to-1.2V, 310nA Quiescent Current, 3fs-FoM Time-Domain Output-Capacitorless LDO with Propagation-Delay-Triggered Edge Detector
Jianming Zhao, Yuan Gao
Agency for Science, Technology and Research, Singapore

S10-3 (1026) 11:20-11:45
A 2-Electrode ECG Amplifier with 0.5% Nominal Gain Shift and 0.13% THD in a 530mV$_{pp}$ Input Common-Mode Range
Jiawei Xu, Zhiliang Hong
Fudan University, China

S10-4 (1121) 11:45-12:10
A Power-Efficient 13-Tap FIR Filter and an IIR Filter Embedded in a 10-Bit SAR ADC
Xin Xin{2}, Linxiao Shen{1}, Xiyuan Tang{1}, Yi Shen{3}, Jueping Cai{3}, Nan Sun{1}
{1}University of Texas at Austin, Armenia; {2}Xi'an University of Posts and Telecommunications, China; {3}Xidian University, China

S10-5 (1136) 12:10-12:35
A Power Efficient ECG Front-End with Input-Adaptive Gain Reaching 67.6-dB Dynamic Range
Liheng Liu, Yanlong Zhang, Li Dong, Youze Xin, Shengwei Gao, Li Geng
Xi'an Jiaotong University, China

Wednesday, November 11

S11 Session: RF Building Blocks

Session date and time: 10:30 – 12:10, November 11, 2020

Session Chairs: Satoshi Tanaka, Murata/Giovanni Mangraviti, imec

S11-1 (1060) 10:30-10:55
A 67fsrms Jitter, −130dBc/Hz In-Band Phase Noise, −256dB FoM Reference Oversampling Digital PLL with Proportional Path Timing Control
Ji-Hwan Seol{2}, Kyojin Choo{2}, David Blaauw{2}, Dennis Sylvester{2}, Taekwang Jang{1}
{1}ETH Zurich, Switzerland; {2}University of Michigan, United States

S11-2 (1115) 10:55-11:20
Digital Evolution of the Quadrature Balanced Power Amplifier Transceiver for Full Duplex Wireless
Nimrod Ginzberg{1}, Dror Regev{2}, Emanuel Cohen{1}
{1}Technion - Israel Institute of Technology, Israel; {2}Toga Networks, a Huawei Company, Israel

S11-3 (1125) 11:20-11:45
An 8.3% Efficiency 96-134 GHz CMOS Frequency Doubler Using Distributed Amplifier and Nonlinear Transmission Line
Shilei Hao{2}, Yi-Wu Tang{3}, Xuan Ding{2}, Li Du{3}, Yuan Du{3}, Adrian Tang{1}, Jane Gu{2}, Mau-Chung Chang{3}
{1}Jet Propulsion Laboratory, United States; {2}University of California, Davis, United States; {3}University of California, Los Angeles, United States

S11-4 (1156) 11:45-12:10
An 8-mW 66-GHz Active Circulator with 40dB TX-RX Isolation in 65nm CMOS for Full-Duplex Radios
Chendi Yu, Howard Luong
Hong Kong University of Science and Technology, Hong Kong

Wednesday, November 11

S12 Session: Circuits and Systems for Emerging Applications

Session date and time: 10:30 – 12:35, November 11, 2020

Session Chairs: Noriyuki Miura, Osaka University/Inhee Lee, University of Pittsburgh

S12-1 (1088) 10:30-10:55
A 40m-Range 90fps CMOS Time-of-Flight Sensor Using SPAD and In-Pixel Time-Gated Pulse Counter
Byungchoul Park, Injun Park, Woojun Choi, Yoondeok Na, Youngcheol Chae
Yonsei University, Korea

S12-2 (1079) 10:55-11:20
A Power-Efficient Current Readout Circuit with VCO-Based 2nd-Order CT ΔΣ ADC for Electrochemistry Acquisition
Hao-Yun Lee, Peng-Wei Huang, Ding-Siang Ciou, Zhan-Xian Liao, Shuenn-Yuh Lee
National Cheng Kung University, Taiwan

S12-3 (1142) 11:20-11:45
A Monolithically Integrated Optical Bandpass Receiver in 0.25µm SiGe BiCMOS Technology for Microwave-Photonic Applications
Giannino Dziallas{1}, Adel Fatemi{1}, Falk Korndörfer{1}, Anna Peczek{4}, Dietmar Kissinger{5}, Lars Zimmermann{3}, Andrea Malignaggi{1}, Gerhard Kahmen{2}
{1} IHP – Leibniz-Institut für innovative Mikroelektronik, Germany; {2 IHP – Leibniz-Institut für innovative Mikroelektronik & Brandenburg Technical University Cottbus, Germany; {3} IHP – Leibniz-Institut für innovative Mikroelektronik & Technical University Berlin, Germany; {4}IHP Solutions GmbH, Germany; {5}Ulm University, Germany

S12-4 (1089) 11:45-12:10
A Wireline Termination Embedded Energy Harvesting System with 300-µW Extracted
Yu-Hong Yang, Tai-Cheng Lee
National Taiwan University, Taiwan

S12-5 (1152) 12:10-12:35
A 8-Channel Rectifier-Free SECE Circuit with 15nA/ch Quescient Current and 580% Efficiency Improvement for Ambient Vibration Energy Harvesting with Broadband MEMS PET Array
Jianming Zhao, Yuan Gao, Beibei Han, Minh Sang Nguyen, Zhipeng Ding, Hyun Kee Chang
Agency for Science, Technology and Research, Singapore

Wednesday, November 11

S13 Session: Bandgap and Temperature Sensors

Session date and time: 13:40 – 15:20, November 11, 2020

Session Chairs: Wanyuan Qu, Zhejiang University/Milin Zhang, Tsinghua University

S13-1 (1133) 13:40-14:05
A 0.0082mm², 192nW Single BJT Branch Bandgap Reference in 0.18µm CMOS
Myungjun Kim, Seonghwan Cho
KAIST, Korea

S13-2 (1065) 14:05-14:30
A 0.14 pJ/Conversion Fully Energy-Autonomous Temperature-to-Time Converter for Biomedical Applications
Joanne Si Ying Tan, Jeong Hoan Park, Jiamin Li, Yilong Dong, Kwok Hoe Chan, Ghim Wei Ho, Jerald Yoo
National University of Singapore, Singapore

S13-3 (1077) 14:30-14:55
A 6.4 nW 1.7% Relative Inaccuracy CMOS Temperature Sensor Utilizing Sub-Thermal Drain Voltage Stabilization and Frequency Locked Loop
Teruki Someya{2}, A.K.M. Mahfuzul Islam{1}, Kenichi Okada{2}
{1}Kyoto University, Japan; {2}Tokyo Institute of Technology, Japan

S13-4 (1116) 14:55-15:20
A 950-pW, 39-pJ/Conversion Leakage-Based Temperature-to-Digital Converter with 43mk Resolution
Cheng-Ze Shao, Yu-Te Liao National Chiao Tung University, Taiwan

Wednesday, November 11

S14 Session: SoC for AIoT

Session date and time: 13:40 – 15:20, November 11, 2020

Session Chairs: Pei-Yun Tsai, National Central Univ, Taiwan/Kazutami Arimoto, Okayama Prefectural Univ.

S14-1 (1002) 13:40-14:05
Fully-Synthesizable All-Digital Unified Dynamic Entropy Generation, Extraction and Utilization Within the Same Cryptographic Core
Sachin Taneja, Massimo Alioto
National University of Singapore, Singapore

S14-2 (1059) 14:05-14:30
CompAcc: Efficient Hardware Realization for Processing Compressed Neural Networks Using Accumulator Arrays
Zexi Ji{2}, Wanyeong Jung{1}, Jongchan Woo{2}, Khushal Sethi{2}, Shih-Lien Lu{3}, Anantha Chandrakasan{2}
{1}KAIST, Korea; {2}Massachusetts Institute of Technology, United States; {3}Taiwan Semiconductor Manufacturing Company, Limited, Taiwan

S14-3 (1084) 14:30-14:55
0.5V 4.8 pJ/SOP 0.93μW Leakage/Core Neuromorphic Processor with Asynchronous NoC and Reconfigurable LIF Neuron
Vishnu Paramasivam Nambiar{1}, J. Pu{2}, Yun Kwan Lee{1}, Aarthy Mani{1}, Tao Luo{1}, Liwei Yang{1}, Eng Kiat Koh{1}, Ming Ming Wong{1}, Fei Li{1}, W. L. Goh{2}, Anh Tuan Do{1}
{1}Agency for Science, Technology and Research, Singapore; {2}Nanyang Technological University, Singapore

S14-4 (1149) 14:55-15:20
A 16/64 QAM Baseband SoC for mm-Wave Transceiver with Self-Healing for FD/FI IQ Mismatch, LO Leakage and CFO/SCO/PNC
Hung-Chih Liu{2}, Hsun-Wei Chan{2}, Henry Lopez{2}, Kang-Lun Chiu{2}, Chih-Wei Jen{2}, Ngoc-Giang Doan{2}, Zheng-Chun Huang{2}, Hsin-Ting Chang{2}, Nien-Hsiang Chang{3}, Pei-Yun Tsai{1}, Yen-Cheng Kuan{2}, Shyh-Jye Jou{2}
{1}National Central University, Taiwan; {2}National Chiao Tung University, Taiwan; {3}TSRI National Applied Research Laboratories, Taiwan

Wednesday, November 11

S15 Session: Wireline Transceiver Techniques

Session date and time: 13:40 – 15:20, November 11, 2020

Session Chairs: Ziqiang Wang, Tsinghua University/Tetsuya Iizuka, University of Tokyo

S15-1 (1042) 13:40-14:05

A 6.4-11 Gb/s Wide-Range Referenceless Single-Loop CDR with Adaptive JTOL

Hye-Ran Kim{2}, Jun-Yeol Lee{1}, Jeong-Su Lee{1}, Dong-Seok Kang{1}, Jung-Hoon Chun{1},
{1}Sungkyunkwan University, Korea; {2}Sungkyunkwan University and Samsung Electronics Co., Ltd., Korea

S15-2 (1083) 14:05-14:30

A Jitter-Tolerant Referenceless Digital-CDR for Cellular Transceivers

Jaekwon Kim{2}, Youngjun Ko{1}, Jahoon Jin{2}, Jaehyuk Choi{2}, Jung-Hoon Chun{2}
{1}Samsung Electronics Co., Ltd., Korea; {2}Sungkyunkwan University, Korea

S15-3 (1064) 14:30-14:55

A 0.4-1.7GHz Wide Range Fractional-N PLL Using a Transition-Detection DAC for Jitter Reduction

Jaekwang Yun, Sangyoon Lee, Yong-Un Jeong, Shin-Hyun Jeong, Suhwan Kim
Seoul National University, Korea

S15-4 (1123) 14:55-15:20

A 50 Gb/s PAM-4 Transmitter with Feedforward Equalizer and Background Phase Error Calibration

Yu-Ting Lin, Wei-Zen Chen National Chiao Tung University, Taiwan

Wednesday, November 11

S16 Session: High-Speed and Low-Power Techniques for SAR-Based ADCs

Session date and time: 15:50 – 17:05, November 11, 2020

Session Chairs: Zule Xu, University of Tokyo/Yong Lim, Samsung Electronics

S16-1 (1061) 15:50-16:15

A 65.5dB SNDR 8.1-11.1nW ECG SAR ADC with Adaptive Latching OSC Based Comparator and DAC Calibration

Kejin Li, Wai-Hong Zhang, Yan Zhu, Chi-Hang Chan, Rui Paulo Martins
University of Macau, Macau

S16-2 (1145) 16:15-16:40

A 10-b 900-MS/s Single-Channel Pipelined-SAR ADC Using Current-Mode Reference Scaling

Kang-Il Cho, Ho-Jin Kim, Jun-Ho Boo, Yong-Sik Kwak, Jun-Sang Park, Seung-Hoon Lee, Gil-Cho Ahn Sogang University, Korea

S16-3 (1105) 16:40-17:05

A 2.2mW 12-Bit 200MS/s 28nm CMOS Pipelined SAR ADC with Dynamic Register-Based High-Speed SAR Logic

Jun-Sang Park, Je-Min Jeon, Jun-Ho Boo, Jae-Hyuk Lee, Kang-Il Cho, Ho-Jin Kim, Gil-Cho Ahn, Seung-Hoon Lee
Sogang University, Korea

Wednesday, November 11

S17 Session: Biomedical & Bioinspired SoCs

Session date and time: 15:50 – 17:30, November 11, 2020

Session Chairs: Yun Chen, Fudan University, China/Jun Zhou, University of Electronic Science and Technology of China

S17-1 (1048) 15:50-16:15

Improved Design and in Vivo Animal Tests of Bone-Guided Cochlear Implant Microsystem with Monopolar Biphasic Multiple Stimulation and Neural Action Potential Acquisition

Sung-Hao Wang{2}, Yu-Kai Huang{2}, Ching-Yuan Chen{2}, Chia-Fone Lee{1}, Chia-Hsiang Yang{3}, Chung-Chih Hung{2}, Chien-Hao Liu{3}, Ming-Dou Ker{2}, Chung-Yu Wu{2}
{1}Hualian Tzu Chi Hospital, Taiwan; {2}National Chiao Tung University, Taiwan; {3}National Taiwan University, Taiwan

S17-2 (1158) 16:15-16:40

A 1.02 μW STT-MRAM Based DNN ECG Arrhythmia Monitoring SoC with Leakage-Based Delay MAC Unit

Kyoung-Rog Lee{1}, Jihoon Kim{1}, Changhyeon Kim{1}, Donghyeon Han{1}, Juhyoung Lee{1}, Jinsu Lee{1}, Hongsik Jeong{2}, Hoi-Jun Yoo{1}
{1}KAIST, Korea; {2}Ulsan National Institute of Science and Technology, Korea

S17-3 (1062) 16:40-17:05

Always-On, Sub-300-nW, Event-Driven Spiking Neural Network Based on Spike-Driven Clock-Generation and Clock- and Power-Gating for an Ultra-Low-Power Intelligent Device

Dewei Wang{1}, Pavan Kumar Chundi{1}, Sung Justin Kim{1}, Minhao Yang{1}, Joao Cerqueira{1}, Joonsung Kang{2}, Seungchul Jung{2}, Sangjoon Kim{2}, Mingoo Seok{1}
{1}Columbia University, United States; {2}Samsung Electronics Co., Ltd., Korea

S17-4 (1082) 17:05-17:30

A 17.7-pJ/Cycle ECG Processor for Arrhythmia Detection with High Immunity to Power Line Interference and Baseline Drift

Yue Yin{2}, Syed Muhammad Abubakar{2}, Songyao Tan{2}, Hanjun Jiang{2}, Zhihua Wang{2}, Seng-Pan U{3}, Wen Jia{1}
{1}Research Institute of Tsinghua University in Shenzhen, China; {2}Tsinghua University, China; {3}University of Macau, Macau

Wednesday, November 11

S18 Session: Intelligent Memory & AI/ML-Assisted Biomedical SoCs

Session date and time: 15:50 – 17:30, November 11, 2020

Session Chairs: Ken Takeuchi, University of Tokyo/Chao Wang, Huazhong University of Science and Technology

S18-1 (1056) 15:50-16:15

Broad-Purpose In-Memory Computing for Signal Monitoring and Machine Learning Workloads

Saurabh Jain, Longyang Lin, Massimo Alioto
National University of Singapore, Singapore

S18-2 (1144) 16:15-16:40

A Dual-Mode Ground-Referenced Signaling Transceiver with a 3-Tap Feed-Forward Equalizer for Memory Interfaces

Jun-Yeol Lee{1}, Hye-Ran Kim{2}, Sanghyeon Park{1}, Jung-Hoon Chun{1}
{1}Sungkyunkwan University, Korea; {2}Sungkyunkwan University and Samsung Electronics Co., Ltd., Korea

S18-3 (1078) 16:40-17:05

Wireless Charging EEG Monitoring SoC with AI Algorithm-Driven Electrical and Optogenetic Stimulation for Epilepsy Control

Zhan-Xian Liao{2}, Yao-Tse Chang{2}, Chieh Tsou{2}, Po-Hao Cheng{2}, Hao-Yun Lee{2}, Peng-Wei Huang{2}, Shuenn-Yuh Lee{2}, Chou-Ching Lin{3}, Gia-Shing Shieh{1}
{1}Ministry of Health and Welfare Tainan Hospital, Taiwan; {2}National Cheng Kung University, Taiwan; {3}National Cheng Kung University Hospital, Taiwan

S18-4 (1151) 17:05-17:30

A 186μW Glucose Monitoring SoC Using Near-Infrared Photoplethysmography

Aminah Hina, Wala Saadeh
Lahore University of Management Sciences, Pakistan

Wednesday, November 11

Special Q&A Session

Session date and time: 18:30 - 19:30, November 11, 2020

This session provides all participants an opportunity to verbally with the authors in the virtual rooms separated by sessions of S10 through S18 on November 11.
The track E which shows 1.5-minute summary presentation helps to give essence of each presentation for those who do not listen to the presentations on that day,
All authors of the following sessions join their rooms.

S10 Analog Techniques
S11 RF Building Blocks
S12 Circuits and Systems for Emerging Applications
S13 Bandgap and Temperature Sensors
S14 SoC for AIoT
S15 Wireline Transceiver Techniques
S16 High-Speed and Low-Power Techniques for SAR-Based ADCs
S17 Biomedical & Bioinspired SoCs
S18 Intelligent Memory & AI/ML-Assisted Biomedical SoCs

Author Index

F

G

H

I

J

K

L

M

N

O

P

R

S

T

U

W

X

Y

Z

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