# A-SSCC 2020 Program-at-a-glance
## November 9-11, 2020 (JST, UCT+9)

| Day | Date | Time(JST) | Track A | Track B | Track C | Track D | Track E |
|---|---|---|---|---|---|---|---|
| 1st Day | Mon., Nov. 9 | 9:00-10:30 | Live Tutorial I<br>Sparsity-Aware Machine Learning Processor | | | Recorded movie<br>SDC Exhibition/ FPGA Demo | Recorded 1.5-min movie<br>presentation by regular speakers |
| | | 10:30-10:50 | Break | | | | |
| | | 10:50-12:20 | Live Tutorial II<br>Ultra-Low-Power DTC-Based Fractional-N Digital PLL Techniques | | | | |
| | | 12:20-13:40 | Lunch Break | | | | |
| | | 13:40-15:10 | Live Tutorial III<br>Introduction to Silicon Photonics Systems and Their Modeling | | | | |
| | | 15:10-15:30 | Break | | | | |
| | | 15:30-17:00 | Live Tutorial IV<br>Integrated Security Interface Against Cyber-Physical Attacks | | | | |
| | | 17:00-18:45 | Break | | | | |
| | | 18:45-19:00 | TPC Meeting | | | | |
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| 2nd Day | Tue., Nov. 10 | 9:00-9:20 | Live Opening Ceremony/ Welcome Remarks | | | Recorded movie<br>SDC Exhibition/ FPGA Demo | Recorded 1.5-min movie<br>presentation by regular speakers |
| | | 9:20-10:05 | Live Session 1 - Plenary Talk 1<br>AI Semiconductor and Intelligent Society<br>Kiyoung Choi, PhD, Ministry of Science and ICT, Republic of Korea | | | | |
| | | 10:05-10:50 | Live Session 1 - Plenary Talk 2<br>Intelligent Chips and Technologies for AIoT Era<br>Yu-Chin Hsu, PhD, BigObject, Inc. | | | | |
| | | 10:50-11:10 | Break | | | | |
| | | 11:10-12:25 | Live Session 2<br>Industry Program: Low-Power Industry Solutions | Live Session 3<br>AI/ML Accelerators on FPGA | Live Session 4<br>High Resolution ADCs with Linearity Enhancement Techniques | | |
| | | 12:25-13:30 | Live Women-in-Circuits(WiC) & Young Professionals Joint Event | | | | |
| | | 13:30-15:35 | Live Session 5<br>Power Management | Live Session 6<br>Low-Power Digital Circuits & Systems | Live Session 7<br>RF & mm-Wave Chip Systems | | |
| | | 15:35-15:50 | Break | | | | |
| | | 15:50-17:30 | Live Session 8 - Panel<br>What other technologies, together with circuit technology, are necessary for AIoT (AI + IoT) | | | | |
| | | 17:30-18:30 | Break | | | | |
| | | 18:30-19:30 | Live Special Q&A Session 1 (separated rooms by each session 2,3,4,5,6,&7) | | | Live Demo Q&A Session (separated rooms by SDC exhibition/FPGA Demo of 10) | |
| | | 19:30-21:00 | Live Virtual Banquet/Award Ceremony | | | | |
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| 3rd Day | Wed., Nov. 11 | 8:30-9:15 | Live Session 9 - Plenary Talk 3<br>Co-optimization targeting future interconnection<br>Wei Tsao, PhD, Hisilicon | | | | Recorded 1.5-min movie<br>presentation by regular oral speakers |
| | | 9:15-10:00 | Live Session 9 - Plenary Talk 4<br>Supercomputer Fugaku - Co-designed with application developers/researchers -<br>Toshiyuki Shimizu, Fujitsu | | | | |
| | | 10:00-10:30 | Break | | | | |
| | | 10:30-12:35 | Live Session 10<br>Analog Techniques | Live Session 11<br>RF Building Blocks | Live Session 12<br>Circuits and Systems for Emerging Applications | | |
| | | 12:35-13:40 | Lunch Break | | | | |
| | | 13:40-15:20 | Live Session 13<br>Bandgap and Temperature Sensors | Live Session 14<br>SoC for AIoT | Live Session 15<br>Wireline Transceiver Techniques | | |
| | | 15:20-15:50 | Break | | | | |
| | | 15:50-17:30 | Live Session 16<br>High-Speed and Low-Power Techniques for SAR-Based ADCs | Live Session 17<br>Biomedical & Bioinspired SoCs | Live Session 18<br>Intelligent Memory & AI/ML-Assisted Biomedical SoCs | | |
| | | 17:30-18:30 | Break | | | | |
| | | 18:30-19:30 | Live Special Q&A Session 2 (separated rooms by each session 10,11,12,13,14,15,16,17&18) | | | | |